

UNITED STATES PATENT APPLICATION

FOR

METHOD AND APPARATUS FOR WAFER LEVEL TESTING OF
INTEGRATED OPTICAL WAVEGUIDE CIRCUITS

INVENTORS:

DMITRI E. NIKONOV
MARK T. MCCORMACK

PREPARED BY:

CHARLES K. YOUNG
INTEL CORPORATION
2200 MISSION COLLEGE BLVD.
SANTA CLARA, CA 95052-8119

(408) 765-8080

Attorney's Docket No. 42390.P13380

"Express Mail" mailing label number EL821772470US

Date of Deposit: December 26, 2001

I hereby certify that I am causing this paper or fee to be deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 CFR 1.10 on the date indicated above and is addressed to: U.S. Patent and Trademark Office, Post Office Box 2327, Arlington, VQ, 22202

Raquel R. Torres

(Typed or printed name of person mailing paper or fee)

Raquel R. Torres
(Signature of person mailing paper or fee) Date

METHOD AND APPARATUS FOR WAFER LEVEL TESTING OF INTEGRATED OPTICAL WAVEGUIDE CIRCUITS

5 BACKGROUND OF THE INVENTION

1. Field of the Invention

The described invention relates to the field of optical circuits. In particular, the invention relates to an optical probe for testing an optical circuit.

10 2. Description of Related Art

Optical circuits include, but are not limited to, light sources, detectors and/or waveguides that provide such functions as splitting, coupling, combining, multiplexing, demultiplexing, and switching. Planar lightwave circuits (PLCs) are optical circuits that are manufactured and operate in the plane of a wafer. PLC technology is advantageous because it can be used to form many different types of optical devices, such as array waveguide grating (AWG) filters, optical add/drop (de)multiplexers, optical switches, monolithic, as well as hybrid opto-electronic integrated devices. Such devices formed with optical fibers would typically be much larger or would not be feasible at all. Further, PLC structures may be mass produced on a silicon wafer.

Figure 1 is a schematic diagram that shows an example of the current way that planar waveguides 20, 22 are tested. Typically, a PLC wafer is diced and optical fibers, 10, 12 are mounted to the edge of a PLC die. Light is sent in to the PLC structure 5 through one optical fiber 10, and a second optical fiber 12 is used to

detect the light. A photodetector coupled to the second optical probe 12 will detect the power of light transmitted to it.

- If the PLC works properly, then fibers are permanently attached to the PLC, and the PLC is put into a package. However, if the PLC does not work properly, the
- 5 unit is discarded, and the time and effort to dice, fiber mount and to comprehensively test the device are wasted. Thus, a method of testing a planar lightwave circuit at the wafer level or before fiber attach is important.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a schematic diagram that shows an example of the current way that planar waveguides are tested.

- 5 Figure 2 is a cross-sectional schematic diagram of an optical probe used to test a planar lightwave circuit (PLC).

Figure 3 is a 3-dimensional view illustrating one embodiment for testing a PLC wafer using two optical probes.

DETAILED DESCRIPTION

A method of testing a planar lightwave circuit is achieved by coupling an optical probe to the planar lightwave circuit. In one embodiment, a second optical probe is used in combination with the first optical probe to test the planar lightwave circuit by sending and receiving a light beam through the planar lightwave circuit.

Figure 2 is a cross-sectional schematic diagram of an optical probe 130 used to test a planar lightwave circuit (PLC) 105. The PLC 105 comprises a waveguide having a core layer 110, an upper cladding 120, and a lower cladding 122. In one embodiment, the upper cladding 120 is only partially applied at the time that the optical probe 130 is used to test the PLC 105, and one or more additional layers of upper cladding are subsequently applied to the PLC 105. In one embodiment, an upper cladding layer of approximately 1-2 microns provides good optical coupling.

The optical probe 130 is an optical fiber comprising a core 132 and an outer cladding 134. The optical fiber 130 has been side-polished so that the core 132 is exposed. The side-polished optical fiber 130 is coupled to the waveguide core 110. In one embodiment, an index-matching fluid 140 is used to improve the optical coupling between the optical probe 130 and the waveguide core 110.

Figure 3 is a 3-dimensional view illustrating one embodiment for testing a PLC wafer 205 using two optical probes 210, 220. PLC wafer 205 may include several PLC dice. In one embodiment, the testing is done before dicing the wafer or fiber interfacing the dice. A first optical probe 210 is coupled to a first portion of a waveguide of the PLC 205. The first optical probe 210 is coupled, e.g., with an

optical fiber, to a light source 212 such as a laser. The light source 212 provides a light beam to the first optical probe 210, which is evanescently coupled to a first portion of the PLC 205.

5 A second optical probe 220 is coupled to a second portion of the PLC 205, and the second optical probe 220 is also coupled to a photodetector 222. Light transmission between the first portion of the PLC and the second portion of the PLC can now be tested. When the first optical probe 210 couples a light beam into the PLC 205, the light beam is detected through the second optical probe by the photodetector 222, if the PLC 205 is working properly.

10 An alignment stage 230 is used to position the first optical probe 210, and an alignment stage 232 is used to position the second optical probe 220. In one embodiment, each alignment stage 230, 232 provides six degrees of freedom. Thus, the optical probes are able to be aligned with the PLC 205 by modifying, for example, the X, Y, and Z coordinates, as well as pitch, yaw, and roll.

15 As previously mentioned, after functionality of the PLC 205 has been established, an additional layer of upper cladding may then be added to the top surface of the PLC 205.

In addition to the testing methods previously mentioned, this technology can be used for fault isolation or intermediate device debugging capabilities. It can be applied to a whole wafer as well as previously diced and possibly fiber interfaced PLCs if they are found non-optimal in performance. One or more probes with detection and/or transmission capability may be coupled at intermediate positions within the PLC (which would be inaccessible by conventional methods) to measure

20

characteristics of PLC subunits and hence determine the local cause of observed effects for debug, fault isolation, and performance enhancement purposes.

Thus, a method and apparatus for testing a planar lightwave circuit is disclosed. However, the specific embodiments and methods described herein are
5 merely illustrative. Numerous modifications in form and detail may be made without departing from the scope of the invention as claimed below. The invention is limited only by the scope of the appended claims.